CURRENT CLAIMS

A copy of the claims is provided below for the convenience of the Examiner.

1. (Cancelled).

2. (Previously Presented) An integrated circuit, comprising:

an adjustable phase shifter operable to receive a reference signal and introduce a phase shift in the reference signal to produce a phase shifted reference signal;

a phase detector operable to identify a phase difference between the reference signal and the phase shifted reference signal;

a control signal generator operable to:

generate a plurality of control signals, each of the control signals capable of causing the adjustable phase shifter to adjust a magnitude of at least one component value in the adjustable phase shifter, wherein the phase shift introduced by the adjustable phase shifter is based at least partially on the magnitude of the at least one component value in the adjustable phase shifter; and

select one of the control signals, the selected control signal capable of causing the adjustable phase shifter to produce the phase shifted reference signal such that the phase difference attains a specified value; and

an analog filter operable to adjust a magnitude of at least one component value in the analog filter based at least partially on the selected control signal.

PAGE 4/18 * RCVD AT 7/15/2005 4:49:14 PM [Eastern Daylight Time] * SVR:USPTO-EFXRF-1/24 * DNIS:2738300 * CSID:972 628 3619 * DURATION (mm-ss):04-50

3. (Previously Presented) The integrated circuit of Claim 2, wherein:

the analog filter comprises one or more first switches and one or more first components; and

the adjustable phase shifter comprises one or more second switches and one or more second components.

4. (Previously Presented) The integrated circuit of Claim 3, wherein:

the analog filter comprises more first components than first switches; and

the adjustable phase shifter comprises more second components than second switches.

5. (Previously Presented) The integrated circuit of Claim 4, wherein:

the first components in the analog filter comprise a plurality of first capacitors;

the second components in the adjustable phase shifter comprise a plurality of second capacitors;

each of the first capacitors is coupled in series to one of the first switches except the first capacitor having a first minimum capacitance; and

each of the second capacitors is coupled in series to one of the second switches except the second capacitor having a second minimum capacitance, the second minimum capacitance approximately equal to the first minimum capacitance.

PAGE 5/18 * RCVD AT 7/15/2005 4:49:14 PM [Eastern Daylight Time] * SVR:USPTO-EFXRF-1/24 * DNIS:2738300 * CSID:972 628 3619 * DURATION (mm-ss):04-50

6. (Previously Presented) The integrated circuit of Claim 5, wherein:

each of the first capacitors has a capacitance that approximately equals a capacitance of one of the second capacitors; and

one of the second capacitors has a capacitance that is greater than the second minimum capacitance and that does not approximately equal any of the capacitances of the first capacitors.

7. (Previously Presented) The integrated circuit of Claim 4, wherein:

the first components in the analog filter comprise a plurality of first resistors;

the second components in the adjustable phase shifter comprise a plurality of second resistors;

each of the first resistors is coupled in series to one of the first switches except the first resistor having a first maximum resistance; and

each of the second resistors is coupled in series to one of the second switches except the second resistor having a second maximum resistance, the second maximum resistance approximately equal to the first maximum resistance.

PAGE 6/18 * RCVD AT 7/15/2005 4:49:14 PM [Eastern Daylight Time] * SVR:USPTO-EFXRF-1/24 * DNIS:2738300 * CSID:972 628 3619 * DURATION (mm-ss):04-50

8. (Previously Presented) The integrated circuit of Claim 2, further comprising:

a first latch operable to provide the plurality of control signals to the adjustable phase shifter; and

a second latch operable to provide the selected control signal to the analog filter;

wherein the control signal generator is further operable to generate command signals to open and close the first and second latches.

9. (Previously Presented) The integrated circuit of Claim 2, wherein the control signal generator comprises:

an integrating element operable to receive signals representing identified phase differences from the phase detector and produce direct voltage components of the signals;

one of:

a comparator operable to compare the direct voltage components and a reference level and produce output signals based on the comparisons; and

an analog-to-digital converter operable to digitize the direct voltage components; and

a digital signal processor operable to select one of the plurality of control signals based at least partially on one of: the output signals and the digitized direct voltage components.

PAGE 7/18 * RCVD AT 7/15/2005 4:49:14 PM [Eastern Daylight Time] * SVR:USPTO-EFXRF-1/24 * DNIS:2738300 * CSID:972 628 3619 * DURATION (mm-ss):04-50

10. (Previously Presented) A method, comprising:

receiving information identifying a phase difference between a reference signal and a phase shifted reference signal, the phase shifted reference signal produced by an adjustable phase shifter introducing a phase shift in the reference signal;

generating a plurality of control signals, each of the control signals capable of causing the adjustable phase shifter to adjust a magnitude of at least one component value in the adjustable phase shifter, wherein the phase shift introduced by the adjustable phase shifter is based at least partially on the magnitude of the at least one component value in the adjustable phase shifter;

selecting one of the control signals, the selected control signal capable of causing the adjustable phase shifter to produce the phase shifted reference signal such that the phase difference attains a specified value; and

providing the selected control signal to an analog filter, the selected control signal capable of causing the analog filter to adjust a magnitude of at least one component value in the analog filter.

11. (Previously Presented) The method of Claim 10, wherein:

the analog filter comprises one or more first switches and one or more first components;

the adjustable phase shifter comprises one or more second switches and one or more second components; and

the control signals are capable of causing at least some of the first and second switches to open and close.

12. (Previously Presented) The method of Claim 11, wherein:

the analog filter comprises more first components than first switches;

the adjustable phase shifter comprises more second components than second switches.

13. (Previously Presented) The method of Claim 12, wherein:

the first components in the analog filter comprise a plurality of first capacitors;

the second components in the adjustable phase shifter comprise a plurality of second capacitors;

each of the first capacitors is coupled in series to one of the first switches except the first capacitor having a first minimum capacitance; and

each of the second capacitors is coupled in series to one of the second switches except the second capacitor having a second minimum capacitance, the second minimum capacitance approximately equal to the first minimum capacitance.

14. (Previously Presented) The method of Claim 13, wherein:

each of the first capacitors has a capacitance that approximately equals a capacitance of one of the second capacitors; and

one of the second capacitors has a capacitance that is greater than the second minimum capacitance and that does not approximately equal any of the capacitances of the first capacitors.

PAGE 9/18 * RCVD AT 7/15/2005 4:49:14 PM [Eastern Daylight Time] * SVR:USPTO-EFXRF-1/24 * DNIS:2738300 * CSID:972 628 3619 * DURATION (mm-ss):04-50

15. (Previously Presented) The method of Claim 12, wherein:

the first components in the analog filter comprise a plurality of first resistors;

the second components in the adjustable phase shifter comprise a plurality of second resistors;

each of the first resistors is coupled in series to one of the first switches except the first resistor having a first maximum resistance; and

each of the second resistors is coupled in series to one of the second switches except the second resistor having a second maximum resistance, the second maximum resistance approximately equal to the first maximum resistance.

16. (Previously Presented) The method of Claim 10, further comprising:

generating command signals to open and close first and second latches, the first latch operable to provide the plurality of control signals to the adjustable phase shifter, the second latch operable to provide the selected control signal to the analog filter.

17. (Previously Presented) The method of Claim 10, wherein receiving information identifying the phase difference and selecting one of the control signals comprise:

receiving signals representing the identified phase differences;

producing direct voltage components of the signals;

one of:

comparing the direct voltage components and a reference level to produce output signals based on the comparisons; and

digitizing the direct voltage components; and

selecting one of the plurality of control signals based at least partially on one of: the output signals and the digitized direct voltage components.

PAGE 11/18 * RCVD AT 7/15/2005 4:49:14 PM [Eastern Daylight Time] * SVR:USPTO-EFXRF-1/24 * DNIS:2738300 * CSID:972 628 3619 * DURATION (mm-ss):04-50

18. (Previously Presented) A computer program embodied on a computer readable medium and operable to be executed, the computer program comprising computer readable program code for:

receiving information associated with a phase difference between a reference signal and a phase shifted reference signal generated by an adjustable phase shifter;

generating a plurality of control signals, each of the control signals capable of causing the adjustable phase shifter to adjust a magnitude of at least one component value in the adjustable phase shifter, wherein a phase shift introduced by the adjustable phase shifter is based at least partially on the magnitude of the at least one component value in the adjustable phase shifter;

selecting one of the control signals, the selected control signal capable of causing the adjustable phase shifter to produce the phase shifted reference signal such that the phase difference attains a specified value; and

providing the selected control signal to an analog filter, the selected control signal capable of causing the analog filter to adjust a magnitude of at least one component value in the analog filter.

PAGE 12/18 * RCVD AT 7/15/2005 4:49:14 PM [Eastern Daylight Time] * SVR:USPTO-EFXRF-1/24 * DNIS:2738300 * CSID:972 628 3619 * DURATION (mm-ss):04-50

19. (Previously Presented) The computer program of Claim 18, wherein

the analog filter comprises a plurality of first switches and a plurality of first capacitors;

the adjustable phase shifter comprises a plurality of second switches and a plurality of second capacitors;

each of the first capacitors is coupled in series to one of the first switches except the first capacitor having a first minimum capacitance;

each of the second capacitors is coupled in series to one of the second switches except the second capacitor having a second minimum capacitance, the second minimum capacitance approximately equal to the first minimum capacitance; and

the control signals are capable of causing at least some of the first and second switches to open and close.

PAGE 13/18 * RCVD AT 7/15/2005 4:49:14 PM [Eastern Daylight Time] * SVR:USPTO-EFXRF-1/24 * DNIS:2738300 * CSID:972 628 3619 * DURATION (mm-ss):04-50

20. (Previously Presented) The computer program of Claim 18, wherein:

the analog filter comprises a plurality of first switches and a plurality of first resistors;

the adjustable phase shifter comprises a plurality of second switches and a plurality of second resistors;

each of the first resistors is coupled in series to one of the first switches except the first resistor having a first maximum resistance;

each of the second resistors is coupled in series to one of the second switches except the second resistor having a second maximum resistance, the second maximum resistance approximately equal to the first maximum resistance; and

the control signals are capable of causing at least some of the first and second switches to open and close.

21. (Previously Presented) The computer program of Claim 18, further comprising computer readable program code for:

generating command signals to open and close first and second latches, the first latch operable to provide the plurality of control signals to the adjustable phase shifter, the second latch operable to provide the selected control signal to the analog filter.